



Figure 1 is a block diagram of a packet processing system. The system takes a **Packet** (1) as input, which is divided into **L2 Info** (2) and **L3 Info** (3). The **L2 Info** (2) is processed by a set of **8 Offset registers** (9), which output **8 x 16bit Rules** (17). The **L3 Info** (3) is processed by a **Determine L3 start; whether tagged or snapped** block (5), which then feeds into a **Parser** (7). The **Parser** (7) outputs **8 x 16bit Masks** (15). The **8 x 16bit Rules** (17) and **8 x 16bit Masks** (15) are combined in an **AND** gate (13) to produce an **8 x 1 bit result** (19). This result (19) is then compared (11) with the **L3 Info** (3) to produce an **8 x 1 bit result** (21). Finally, the **8 x 1 bit result** (21) is combined with the **L3 Info** (3) in a **Combine Results** block (23) to produce the **Final key**.